ABSTRACT

An apparatus for compensating for glitch occurrence in a reset signal that is applied in an integrated circuit, includes: a logic stage capable to process an incoming signal and a delayed incoming signal that is a delayed version of the incoming signal, the logic stage capable to generate an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will be in the same state. An apparatus for compensating for glitch occurrence in a reset signal that is applied in an integrated circuit, includes: a logic stage capable to process an incoming signal and a delayed incoming signal that is a delayed version of the incoming signal, the logic stage capable to generate an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will have a state similar to the state of the incoming signal, and when the incoming signal and the delayed incoming signal are not in the same state, the output signal will have a state similar to a previously sampled state of the incoming signal.